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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/542,649	07/19/2005	Shoji Ito	Q89230	1668

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EXAMINER	
PHAN, THIEM D	

ART UNIT	PAPER NUMBER
3729	

MAIL DATE	DELIVERY MODE
08/21/2008	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/542,649	ITO ET AL.	
	Examiner	Art Unit	
	THIEM PHAN	3729	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *03 July 2008*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-51* is/are pending in the application.

4a) Of the above claim(s) *1-14,20-26 and 28-45* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *15-19,27 and 46-51* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *15 January 2008* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *6/19/08*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Continued Examination Under 37 CFR 1.114

1. A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicants' submission filed on 07/03/08 has been entered.

Claim Rejections - 35 USC § 103

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3. Claims 15-19, 27 and 46-51 are rejected under 35 U.S.C. 103(a) as being unpatentable over Sakamoto et al (US 6,281,446).

Regarding claim 15, Sakamoto et al teach a method of manufacturing a multi-layered circuit board, comprising:

- laminating a base material (Fig. 7A, 16) having a wiring circuit (Fig. 7A, 21) which is formed into a predetermined outer shape with one front surface of a motherboard (Fig. 7B, 11) by positioning the base material on the motherboard, superposing the base

material and the motherboard (Fig. 7A, Arrow); except for describing the heating and the pressing of the base material and the motherboard together.

It would be obvious to one of ordinary skill in the art at the time the invention was made to heat and press the base material and the motherboard together in order to compact them in one single piece, since it is known in the art that a plurality of solder balls to be cured are positioned between the two devices (Col. 7, lines 64 & 65) and the heating with the pressing process is taught in their makings (Col. 7, lines 28-30 & lines 53-55).

Regarding claim 16, Sakamoto et al teach a method of manufacturing a multi-layered circuit board, comprising:

- forming a wiring circuit (Figs. 4A-5B, 13a & bottom end of 11) on at least one of a front surface and a rear surface of the motherboard (Fig. 5B, 11);
- making a via hole (Fig. 5B, 15); and
- laminating a base material (Figs. 6A-7B, 16) having a wiring circuit (Fig. 6B, 18) which is formed into a predetermined outer shape with at least one of a front surface and a rear surface of a motherboard by positioning the base material on the motherboard, superposing the base material and the motherboard (Fig. 7A, Arrow); except for describing the heating and the pressing of the base material and the motherboard together.

It would be obvious to one of ordinary skill in the art at the time the invention was made to heat and press the base material and the motherboard together in order to compact them in one single piece, since it is known in the art that a plurality of solder balls to be cured are positioned between the two devices (Col. 7, lines 64 & 65) and the heating with the pressing process is taught in their makings (Col. 7, lines 28-30 & lines 53-55).

Regarding claim 17, Sakamoto et al teach that an outer shape of the base material (Fig. 7A, 16) having a wiring circuit (Fig. 7A, 18) is smaller than the outer shape of the motherboard (Fig. 7A, 11).

Regarding claim 18, Sakamoto et al teach the forming of a cover layer (Fig. 4A, 39) having an opening (Figs. 4A-7B, 15a) for positioning the base material (Fig. 7A, 16) having a wiring circuit (Fig. 7A, 18) prior to the operation of laminating (Figs. 7A & 7B, 16 & 11) the base material having a wiring circuit with the motherboard.

Regarding claim 19, Sakamoto et al teach a method of manufacturing a multi-layered circuit board including the laminating of the base material (Fig. 1, 16) having a wiring circuit (Fig. 1, 18) with the motherboard (Fig. 1, 11), the filling up of the cavity (Fig. 1, 15; col. 5, lines 12-16) with resin, which reads on applicants' claimed invention; except for forming a cover layer for coating the motherboard and the base material.

It would be obvious to one of ordinary skill in the art at the time the invention was made to form a cover layer for coating the motherboard and the base material, since it is known in the art that the process is to make a printed circuit board safe from the environment (Col. 4, line 4) and that a printed circuit board must always be covered with a silkscreen layer at the two front and rear exposed surfaces, except at the contact pads for soldering or connector insertion, to protect against flux during reflow and contaminants from environment.

Regarding claim 27, Sakamoto et al teach the laminating of a base material with single-sided wiring circuit (Fig. 12A, 19b), which is formed into a predetermined outer shape (Fig. 13A, 33) to one frontal surface of the motherboard (Fig. 13A, 31) by positioning the base material on

the motherboard, superposing the base material and the motherboard (Fig. 7A, Arrow); except for describing the heating and the pressing of the base material and the motherboard together.

It would be obvious to one of ordinary skill in the art at the time the invention was made to heat and press the base material and the motherboard together in order to compact them in one single piece, since it is known in the art that a plurality of solder balls to be cured are positioned between the two devices (Col. 7, lines 64 & 65) and the heating with the pressing process is taught in their makings (Col. 7, lines 28-30 & lines 53-55).

Regarding claims 46, 48 and 50, as best understood, Sakamoto et al teach a motherboard or base board (Fig. 1, 11a) of substantially solid layer.

Regarding claims 47, 49 and 51, Sakamoto et al teach that the location of the base material (Fig. 7A, 16) is dictated by the circuit layout (Fig. 7A, 22) of the motherboard (Fig. 7A, 11).

Response to Arguments

4. Applicants' arguments with respect to claims 15, 16 and 27 have been considered but are moot in view of the new ground(s) of rejection.

Furthermore, applicants' assertions (Remarks, page 20, 1st paragraph) of the benefits of minimizing waste or maximizing flexibility in designing multilayered board are not claimed.

Conclusion

5. The prior art made of record and not relied upon is considered pertinent to applicants' disclosure.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Tim Phan whose telephone number is 571-272-4568. The examiner can normally be reached on M & Tu, 6AM - 2PM, and W & Th, 9AM – 5PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Peter Vo can be reached on 571-272-4690. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

/Phan Thiem/

Tim Phan
Examiner
Art Unit 3729

August 18, 2008